Logo

Description automatically generated**EEDG/CE 6370**

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**Design and Analysis or Reconfigurable Systems**

**Homework 7**

**VGA-FPGA Interface**

**Student Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Part I – VGA implementation with DCM IP to set clock**

a.) Follow the instructions in the lab sheet and implement the design which draws two squares of different color to the screen using Altera’s IP catalogue to create a clock of different frequency (based on screen size and resolution). Create a short video demonstrating the working design

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| Marks |
| 4 |
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b.) Report the number of ALMs, ALUTs and critical path of the design from the synthesis report. Compute the maximum frequency.

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| Marks |
| 2 |
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**Part II – Timing analysis**

c.) Open TimeQuest. 1) Netlist 🡪 Create Timing netlist. 2.) Read .sdc file from VGA project (Constraints 🡪 read sdc file). 3.) Update timing netlist (Netlist 🡪 Update Timing netlist)

Report the slack of the circuit. Is it positive or negative? Explain what that means (Reports 🡪 slack 🡪 Report setup summary and Report hold summary.

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| Marks |
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e.) Reporting the skew. Task pane 🡪 Custom reports 🡪 report skew. Edit “From clock” and “To clock” combo boxes. Which clocks should you choose? Explain why.

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f.) Is the slack positive or negative? What does the slack result obtained suggests?

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| Marks |
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**Part III – Power Estimation**

1. Use the PowerPlay Excel sheet to estimate the total power of the design. Enter manually the resources used. Let the toggle rate at its default value. Annotate the estimated dynamic and static power, with the following values. Discuss the results.

(6 marks)

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| --- | --- | --- | --- | --- | --- | --- |
| Configs | Frequency  [MHz] | Temperature [oC] | Toggle rate [%] | Static power (Quiescent) [W] | Dynamic Power [W] | Total Power [W] |
| Config 1 | 50 | 50 | 12.5 |  |  |  |
| Config 2 | 60 | 50 | 12.5 |  |  |  |
| Config 3 | 70 | 50 | 12.5 |  |  |  |
| Config 4 | 50 | 55 | 12.5 |  |  |  |
| Config 5 | 50 | 60 | 12.5 |  |  |  |
| Config 6 | 50 | 65 | 12.5 |  |  |  |
| Config 7 | 50 | 50 | 13.75 |  |  |  |
| Config 8 | 50 | 50 | 15 |  |  |  |
| Config 9 | 50 | 50 | 16.25 |  |  |  |

Compare the results obtained from Power Play Early Power Estimator (Excel spreadsheet) with the results obtained from Power Play Power Analyzer (Quartus II power estimation tool). Do the results match? Explain why yes/no.

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| Marks |
| 4 |
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**Part IV – Re-doing VGA Output**

h.) Re-do the design and display a red 4cm2 square (2cm x 2 cm) on a white background (full display) at the center of the display. Write down the ‘if’ condition from the VHDL ‘hw\_image\_generator’ that allows the printing of the red square (code snippet. Adjust the monitor size parameters (porch values and horizontal and vertical pixels, etc..). Include the parameters settings here and a screenshot of the working design.

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| Marks |
| 4 |
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**Bonus:**

Modify the design so that you write on the screen: ‘UT Dallas’. Append your code here (only the newly added code)

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| Marks |
| 5 bonus |
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